WHAT IS CLAIMED IS:

1. A voltage controlled oscillator (VCO) capable of receiving a +V(IN) control voltage and a -V(IN) control voltage and outputting a VCO output signal having a frequency of oscillation determined by said +V(IN) control voltage and said -V(IN) control voltage, said VCO comprising:

a storage capacitor capable of being charged linearly by a constant charge current and discharged linearly by a constant discharge current;

a comparator capable of comparing a voltage on said storage capacitor to an upper threshold voltage and a lower threshold voltage, wherein an output of said comparator drops to a negative saturation voltage (-V(SAT)) when said storage capacitor voltage rises above said upper threshold voltage and said comparator output rises to a positive saturation voltage (+V(SAT)) when said storage capacitor voltage drops below said lower threshold voltage;

a constant charge current source capable of injecting said constant charge current to said storage capacitor when said comparator output rises to said positive saturation voltage; and

a constant discharge current source capable of draining said constant discharge current from said storage capacitor when

said comparator output drops to said negative saturation voltage.

2. The voltage controlled oscillator (VCO) as set forth in Claim 1 wherein said comparator output is coupled to said VCO output.

3. The voltage controlled oscillator (VCO) as set forth in Claim 2 wherein said constant charge current is determined by said +V(IN) control voltage.

4. The voltage controlled oscillator (VCO) as set forth in Claim 3 wherein said constant discharge current is determined by said -V(IN) control voltage.

5. The voltage controlled oscillator (VCO) as set forth in Claim 4 wherein said constant charge current source comprises a PNP-type bipolar junction transistor having a base coupled to said +V(IN) control voltage, an emitter coupled to said comparator output via a load resistor, and a collector coupled to said storage capacitor.

6. The voltage controlled oscillator (VCO) as set forth in Claim 5 wherein said constant charge current source comprises a NPN-type bipolar junction transistor having a base coupled to said -V(IN) control voltage, an emitter coupled to said comparator output via said load resistor, and a collector coupled to said storage capacitor.

7. The voltage controlled oscillator (VCO) as set forth in Claim 6 wherein said comparator comprises: 1) an operational amplifier having an inverting input coupled to said storage capacitor; 2) a first resistor (R1) having a first terminal coupled to ground and a second terminal coupled to a non-inverting input of said operational amplifier; and 3) a second resistor (R2) having a first terminal coupled to an output of said operational amplifier and a second terminal coupled to said non-inverting input of said operational amplifier, wherein said operational amplifier output comprises said comparator output.

8. The voltage controlled oscillator (VCO) as set forth in Claim 7 wherein said upper threshold voltage is determined by the product: [(R1)/(R1+R2)][+V(SAT)].

9. The voltage controlled oscillator (VCO) as set forth in Claim 7 wherein said lower threshold voltage is determined by the product: [(R1)/(R1+R2)][-V(SAT)].

10. The voltage controlled oscillator (VCO) as set forth in Claim 6 wherein said constant charge current is determined by a difference between said positive saturation voltage and said +V(IN) control voltage and constant discharge current is determined by a difference between said negative saturation voltage and said -V(IN) control voltage.

11. A processing system comprising:

a clocked circuit capable of operating at very low frequency using an external clock signal; and

a phase-locked loop (PLL) coupled to said clocked circuit capable of supplying said external clock signal with high linearity at very low frequency, said PLL comprising:

a frequency divider circuit for dividing a frequency of said external clock signal by N;

a phase detector capable of detecting a phase difference between a frequency divided output of said frequency divider circuit and an input reference signal and generating therefrom a phase difference signal;

a charge pump and loop filter circuit capable of converting said phase difference signal to a +V(IN) control voltage and a -V(IN) control voltage; and

a voltage controlled oscillator (VCO) capable of receiving said +V(IN) control voltage and said -V(IN) control voltage and outputting a VCO output signal having a frequency of oscillation determined by said +V(IN) control voltage and said -V(IN) control voltage, said VCO comprising:

a storage capacitor capable of being charged linearly by a constant charge current and discharged

linearly by a constant discharge current;

a comparator capable of comparing a voltage on said storage capacitor to an upper threshold voltage and a lower threshold voltage, wherein an output of said comparator drops to a negative saturation voltage (-V(SAT)) when said storage capacitor voltage rises above said upper threshold voltage and said comparator output rises to a positive saturation voltage (+V(SAT)) when said storage capacitor voltage drops below said lower threshold voltage;

a constant charge current source capable of injecting said constant charge current to said storage capacitor when said comparator output rises to said positive saturation voltage; and

a constant discharge current source capable of draining said constant discharge current from said storage capacitor when said comparator output drops to said negative saturation voltage.

12. The processing system as set forth in Claim 11 wherein said comparator output is coupled to said VCO output.

13. The processing system as set forth in Claim 12 wherein said constant charge current is determined by said +V(IN) control voltage.

14. The processing system as set forth in Claim 13 wherein said constant discharge current is determined by said -V(IN) control voltage.

15. The processing system as set forth in Claim 14 wherein said constant charge current source comprises a PNP-type bipolar junction transistor having a base coupled to said +V(IN) control voltage, an emitter coupled to said comparator output via a load resistor, and a collector coupled to said storage capacitor.

16. The processing system as set forth in Claim 15 wherein said constant charge current source comprises a NPN-type bipolar junction transistor having a base coupled to said -V(IN) control voltage, an emitter coupled to said comparator output via said load resistor, and a collector coupled to said storage capacitor.

17. The processing system as set forth in Claim 16 wherein said comparator comprises: 1) an operational amplifier having an inverting input coupled to said storage capacitor; 2) a first resistor (R1) having a first terminal coupled to ground and a second terminal coupled to a non-inverting input of said operational amplifier; and 3) a second resistor (R2) having a first terminal coupled to an output of said operational amplifier and a second terminal coupled to said non-inverting input of said operational amplifier, wherein said operational amplifier output comprises said comparator output.

18. The processing system as set forth in Claim 17 wherein said upper threshold voltage is determined by the product: [(R1)/(R1+R2)][+V(SAT)].

19. The processing system as set forth in Claim 17 wherein said lower threshold voltage is determined by the product: [(R1)/(R1+R2)][-V(SAT)].

20. The processing system as set forth in Claim 16 wherein said constant charge current is determined by a difference between said positive saturation voltage and said +V(IN) control voltage and constant discharge current is determined by a difference between said negative saturation voltage and said -V(IN) control voltage.